DISCIPLINE SPECIFIC ELECTIVES (DSE-5)

CREDIT DISTRIBUTION, ELIGIBILITY AND PRE-REQUISITES OF THE COURSE

Course title & Code	Credits	Credit distribution of the course			Eligibility criteria	Pre-requisite of the course (if any)
		Lecture	Tutorial	Practical/ Practice		
CMOS Digital VLSI Design ELDSE7E	4	3	-	1	Class XII passed with Physics + Mathematics/Applied Mathematics + Chemistry OR Physics + Mathematics/Applied Mathematics + Computer Science/Informatics Practices	Digital Electronics, Analog Electronics-I & II, Basic VLSI Design

Learning Objectives

This course introduces the student to develop the ability to design and analyze combinational and sequential digital circuits using VHDL/Verilog; design methodologies of memory circuits such as SRAM and DRAM; acquire hands-on skills in layout design and to simulate and analyze VLSI circuits, including post-layout simulations

Learning outcomes

On successful completion of this course, students will be able to:

- Design and analyze CMOS-based combinational and sequential circuits, focusing on performance metrics like power, delay, and reliability.
- Design and evaluate memory circuits, including SRAM and DRAM, considering trade-offs in stability, speed, and power.
- Demonstrate proficiency in creating and verifying layouts of digital circuits, ensuring adherence to design rules and industry standards.
- Utilize EDA tools for circuit design, simulation, and layout verification.

SYLLABUS OF ELDSE-7E **Total Hours- Theory: 45 Hours, Practicals: 30 Hours**

UNIT – I (12 Hours)

HDL: History of HDL; Structure of VHDL; VHDL Modules : entity, architectures, concurrent signal assignment; Data Flow Modelling, Structural Modelling, Behavioural Modelling.

UNIT – II (14 Hours)

Verilog: Verilog/VHDL Comparisons; Module, Data Types, Operators and Expressions, Instantiation and Hierarchical Design, Blocking and Non-Blocking Assignments, Gate Level, Dataflow and Behavioural Modelling, RTL, Verilog Tasks and Functions, Design Flow and Verilog Test Bench

UNIT – III (10 Hours)

SRAM and DRAM : 6T SRAM cell design and read & write-operation, stability analysis and noise margins, stick diagram of a traditional 6T SRAM cell, DRAM architecture and refresh mechanism, DRAM Architecture - One-transistor, Three-transistor and Four-Transistor DRAM cell, DRAM subarray -Open and Folded Bitlines.

UNIT – IV (09 Hours)

Layout Design Rules and DRC : basic layout design rules, metal layers, contacts, and vias in CMOS layouts, design rule checks, layout versus schematic, Inverter Cell Layout. Introduction to - post-layout simulation; parasitic extraction; full-custom layout design; concept of standard cell & parameterized cells; importance of VLSI CAD tools; ASIC design flow vs. FPGA flow.

Practical component (if any) – Digital VLSI Design Lab

(Practicals to be performed using VHDL/Verilog, Ngspcie/LTspice/QUCS, kiCAD/MagicVLSI, XCircuit, OpenRAM, CADENCE/MENTOR GRAPHICS)

Learning outcomes

The Learning Outcomes of this course are as follows:

- Apply VHDL/Verilog to design the Digital Circuits
- Get familiarized with the VLSI design Simulation Tools
- Create Layout of a CMOS inverter and perform design rule checks (DRC).

LIST OF PRACTICALS (Total Practical Hours- 30 Hours)

1. Design Full Adder/Subtractor using VHDL.
2. Design a Counter using VHDL.
3. Design MUX/Multiplier Circuit using Verilog
4. Design ALU using Verilog
5. Design a 6T SRAM cell, simulate its read/write operation.

6. Draw the stick diagram for a CMOS inverter and basic gates like NAND and NOR.
7. Create the layout of a CMOS inverter, ensuring compliance with basic design rules. Perform design rule checks (DRC).
8. Perform post-layout simulation for a CMOS inverter, including parasitic extraction. Analyze the impact of parasitics on circuit performance.

Note: Students shall sincerely work towards completing all the above listed practicals for this course. In any circumstance, the completed number of practicals shall not be less than seven.

Essential/recommended readings

1. J. Bhasker, A Verilog® HDL Primer, BSP, 3rd Edition, 2024, ISBN: 9788178001425
2. Samir Palnitkar: Verilog HDL-A guide to digital design and synthesis-, Pearson, 2003, ISBN- 0-13-044911-3 / 978-0130449116
3. Wayne Wolf: Modern VLSI Design: IP-Based Design, PHI, 4th Edition, 2015, ISBN-9780137145003
4. Weste and Harris: CMOS VLSI Design: Circuits and Systems Perspective, Pearson/Addison-Wesley,4th Edition, 2010, ISBN- 9780321547743
5. Kang and Lebelbigi: CMOS Digital IC Circuit Analysis and Design, McGraw-Hill Education, 4th Edition, 2014, ISBN- 9780073380629

Suggestive readings

1. Jan M. Rabaey, Anantha Chandrakasan, and Borivoje Nikolic: Digital Integrated Circuits: A Design Perspective, Prentice Hall Electronics, 2003, ISBN-10 0130909963; ISBN-13 978-0130909961
2. Randall L. Geiger, Phillip E. Allen, and Noel R. Strader: VLSI Design Techniques for Analog and Digital Circuits, McGraw Hill, 1989, ISBN-10 0070232539; ISBN-13 978-0070232532

Note: Examination scheme and mode shall be as prescribed by the Examination Branch, University of Delhi, from time to time.